International Journal of Advanced Computer Technology (IJACT)

ISSN:2319-7900

FPGA based image acquisition and graphic interface for hardness tests by indentation

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Abstract

We present a real-time video and image acquisition system, which has important characteristics such as modularity, configurability, versatility, and low cost. This system was developed on the Altera DE2 Board® using Verilog HDL® (Hardware Description Language), VHDL® (VHSIC Hardware Description Language) and Block Diagram as coding languages. The proposed system architecture was applied for real-time image acquisition for hardness tests by indentation, using a specific microdurometer and a CCD camera. Our system provides an instrument for real-time image processing and evaluation controlled from a host computer, that is, for improvement and automatization of the evaluation of indentation footprints which traditionally has been performed by human operators. In addition, our system controls the image acquisition through graphic interface for storing the images with JPG or BMP format. The graphic interface was design using Delphi software and includes an algorithm to implement different configurations of infinite impulse response filters. Thus, the image storage is realized by a combination of software and hardware. Several experiments showed that our system has high real-time performance, stability and robustness with respect to electronic noise.

Keywords— FPGA, graphic interface, image acquisition system, microdurometer, hardness test.

Introduction

The aim of this work is to contribute to the automatization of hardness tests by indentation which are important in quality control in industrial applications, but also in other fields as for example biomedical research and diagnostics. Specially, this article pretends to make possible an analysis of indentation footprints by means of digital image analysis, in research as well as in industrial environments. Instrumented indentation testing has been growing recently, so, one expects new technological developments in this field in the near future.

Hardness tests are commonly performed with the help of durometers, which permit to measure the indentation force and to observe the footprint made by the indenter. Nevertheless, an evaluation manually made is subjective and depends on the point of view of the human operator.

Some researchers have proposed implementations of image acquisition in host computers for the analysis of indentations of types Vickers and Brinell [2,10]. Algorithms based on the Hough transform have been developed to determine the locations of the vertices of the indentation footprint [3,4,8,9]. These systems depend on commercial frame grabbers for image acquisition, and commonly they need to use high cost software such as Labview® or Matlab®. In the biomedical field, a stiffness probe based on force and vision sensing for soft tissue diagnosis applying indentation was presented in [6]. A limitation in such known systems consists in the large time consumed to process a large set of images. This problem is caused by the usage of commercial image processing software on a personal computer (PC), where real-time processing is difficult to be achieved [7].

One alternative is to use a Field Programmable Gate Array (FPGA). Continual growth in the size and functionality of FPGAs over recent years has resulted in an increasing interest in their use as implementation platforms for image acquisition. For example, a research on face recognition was presented in [13], where the usage of the Static memory RAM (SRAM) instead of a Synchronous Dynamic RAM memory (SDRAM) was proposed for uploading more detailed information of the pixels than in applications known before. The FPGA has been recognized as a flexible system which can be used as an open and low cost platform for implementing and testing real-time image processing algorithms [12, 5] in future industrial applications. Nevertheless, many system proposals based on FPGAs need the TRDB-D5M® Camera and the TRDB-LTM® LCD Touch Panel supplied by Terasic [14] to reach its real-time operation, which increases the cost for its future integration on-chip.

The present article proposes a low cost system for real-time acquisition and display of the digital image representing the indentation scene. The future idea is to generate the image at several time moments of the indentation process and then, to study the footprint left by the indenter on the material to be analyzed. In particular, when using an indent-

ISSN:2319-7900

er of pyramidal shape, the extent of the diagonals of the footprint which is basically of rhombus shape, will be of interest. We use the specific Mitutoyo microdurometer model HM-124® [11] which reproduces the images of the indentation scene by an implemented CCD camera. It is important to mention that the indenter measuring system HM-124, that belongs to the HM-100® series, does not have accessories which permit to change its CCD. This can be considered as a limitation for enhancing and optimizing the HM-124 test system. Thus, the HM-124 lacks a commercial frame grabber to be adapted to a host computer. Therefore, this paper deals with the design and realization of image acquisition in real-time for the HM-124, through an implementation in an FPGA Altera Cyclone II 2C35® of the DE2 Board®, using Verilog HDL (Hardware Description Language), VHDL (VHSIC Hardware Description Language) and Block Diagram as coding languages [1]. In addition, our system transfers the data from DE2 SRAM to a host computer (PC) and vice versa through an USB connection, utilizing a graphic interface developed in Delphi Borland 7.net®, which is used to image storage in the host computer in JPG or BMP format. The graphic interfaceincludes an algorithm to implement infinite impulse response filters. Other researchers presented in [17] an image capture and storage system using a SOPC® (System on programmable chip) approach realized on the Altera DE2 platform®. However, they need to increment its logic elements (4572/33216) and memory bits (154200/483840), and they use the NIOS II software® [1] which is more expensive than the DE2 Board.

This paper is organized as follows: In Section 2, we describe the hardness test by indentation by means of microdurometers. In Section 3, we present a new proposal of an image acquisition system based on FPGA. In section 4, contains results and discussions. Conclusions and comments on future research are included in Section 5.

2. HARDNESS TEST BY INDENTATION

In the fabrication process of microelectronic devices, hardness tests are very important for the evaluation of the mechanical properties and quality control of the manufactured devices. For instance, the analysis of residual stresses of thin films on semiconductor substrates is a research issue at the microelectronics industry due to they can damage or reduce the lifetime of the microelectronic devices.

In general, an indentation hardness test consists in applying a punctual static force on the surface of a material to be analyzed during a permanent time and using some specific form of indenter. The result is a footprint on the material surface, as shown in Figure 1. Ceramics, metals, polymers and biological samples are examples of materials that can be analyzed with hardness tests.

As shown in Figure 1, an indenter measuring system that performs a hardness test consists of an indenter with a specific geometry, usually mounted on a rigid column, through which the force towards the sample is applied, an actuator where the force is coming from, and a sensor to measure the displacement of the indenter. Due to recent advances in instrumentation, actual technologies demand a high accuracy in the measurement of mechanical properties, in particular in processes of manufacture of microelectronic circuits and in magnetic field measuring industries [15]. Microdurometers allow to register the force applied to the material as well as to generate the image of the footprint made by the temporal application of the indenter, after having removed the same. These measurements on forces and footprints serve to determine hardness, but they also help in deducing other properties of materials, such as tensile modulus, resilience, plasticity, compression, resistance, elasticity, ductility, flow, and cut tension. For hardness tests in practice applied in nanoindentation of polymers, forces used range from 1N to 300mN (30g) [16]. The resolution of Microdurometers is about 0.2N of force applied and 2nm of displacement of the sample to be submitted to the indenter.

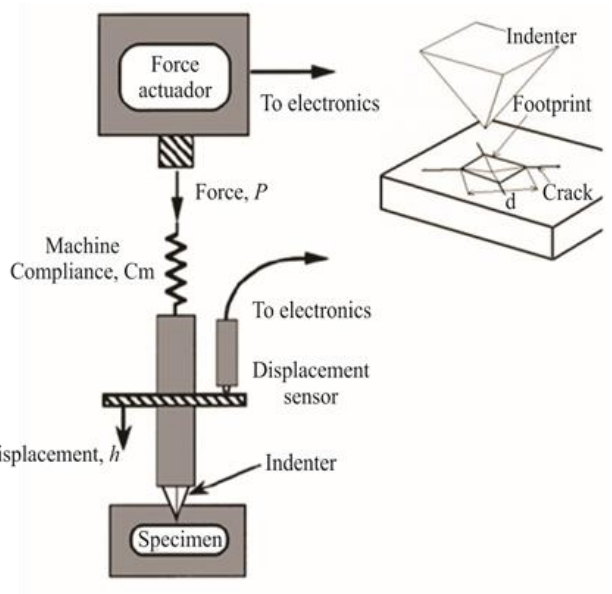

Figure 1. Left: Basic components of an instrumented indentation testing system. Right: Footprint produced by applying a force on a fragile material through an indenter of pyramidal form.

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3. IMAGE ACQUISITION SYSTEM BASED ON FPGA

A. Key features of the image acquisition system

The proposed image acquisition system is embedded and has a real-time performance. The first characteristic allows its integration within a special system or equipment, which will analyze digital images obtained from indentation tests. In consequence, the FPGA is designed to perform image digitization. Real-time image processing is difficult to be achieved on a serial processor. This is due to several factors such as the data set represented by the image, and the complex operations to capture the image. At real-time video rates of 25 frames per second, a single operation performed on every pixel of a 768 by 576 color image (PAL frame) equates to 33 million operations per second. This does not take into account the overhead of storing and retrieving pixel values. Many image-processing applications require several operations on each pixel, which results in an even high number of operations per second.

B. Basic structure of a FPGA

A FPGA consists of the following four parts where each part has specific functions:

- Input and output modules (IOB) of the FPGA, which are used to condition different types of electrical signals, such as audio and video.
- The microprocessor (Logical Unit), which performs all logic functions.
- The Block Ram is dedicated to data storage.
- The Routing Resources deal with connecting the logic unit, the IOB and the Block Ram, to achieve signal transmission.

The development of our image acquisition system based on a FPGA follows a strategy which started with a circuit design, followed by integration, downloading a configuration, and finally a debugging and verification process. For the circuit design, we applied the use of the HDL and the schematic input. The integration step consisted in translating the HDL, the schematic and other design inputs into the logic connection composed by trigger registers, memory blocks and other basic logic units. The circuit design is based on the hardware resources provided by the FPGA and on some aims to be achieved such as speed, power consumption, cost, and circuit types.

C. Hardware description

The image acquisition system proposed in this paper is composed of the following three units: input unit, processors, and output unit. The NTSC (National Television System Committee) format output video given by the camera is the supply for the composite video input port of the Altera's DE2 board. The on-board TV decoder (ADV7181B) converts the analog video format into a raw digital format of the video, which in turn is the supply for the FPGA. This raw digital data is processed through the ITU656 module to provide the required YCbCr (luminosity and chrominance) image components. An YCbCr to RGB (Red-Green-Blue) module is also introduced to convert the pixels into a format that can be visualized on a VGA (Video Graphics Array) screen. As processors, we used the FPGA devices Altera Cyclone II 2C35 NTSC. The processor 2C35 supports the communication with a PC through the JTAG interface. For this reason, Altera has developed the respective software, the DE2 control panel [9], which supports the data transfer from DE2´s SRAM to PC and vice versa through an USB connection from a host computer. Figure 2 shows the block diagram of the Altera Cyclone II 2C35 used in the design and implementation of this work.

The processor Altera Cyclone II 2C35 of the DE2 Board has only one single data rate synchronous dynamic RAM memory chip (SDRAM).Therefore, this dispositive cannot storage images in the host computer (e.g., jpeg or bmp format). A first idea for the implementation of an image digitization system would be to choose the development platform DE2 by Altera, the TRDB-D5M Camera and the NIOS II Software by Terasic as in [9]. However, this can increase substantially the cost for future integration of the system on-chip. To resolve this problem, we designed a graphic interface which is used to image storage in the host computer in JPG or BMP format.

The graphic interface was developed in Delphi®, which uses object-oriented programming techniques to implement algorithms. This graphic interface has advantages such as integrity, compatibility, portability and scalability, which allow the transfer the data from DE2 SRAM® to a host computer (PC) and vice versa through an USB connection.

The graphic interface provides control for two cameras and the parameters of digital signal processing implemented in the FPGA. These parameters depend on the electronic noise of the CCD, the monitor and other devices integrated in the FPGA board.

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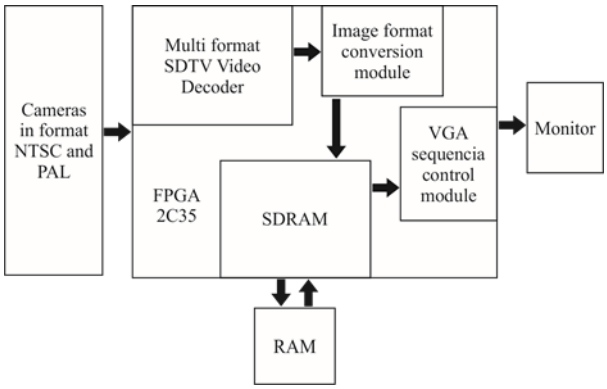

Figure 2. Block diagram of the Altera Cyclone II 2C35 processor, which is used to decode the video from the camera.

In order to find the frequencies in which the electronic noise of the TV decoder output has the maximum values, it is necessary to measure its frequency domain spectrum. For this, a N9020A spectrum analyzer (Agilent Technologies®) is used to evaluate the behavior of the TV decoder output voltage at the frequency domain considering also its higher harmonics, as shown in Figure 3. By using the Fourier series at the TV decoder output, where the frequency spectrum is represented as

$$x(t) = \frac{A}{p} + \frac{A}{4}\cos(w_o t) + \sum_{n=2} \frac{2A}{p}\frac{(-1)^{\frac{n}{2}+1}}{n^2+1}\cos(nw_o t) \quad (1)$$

where ω_o is the fundamental frequency and A is the magnitude of the harmonic. Thus, fundamental signal of the frequency spectrum:

$$\frac{A}{p} = C_o^x \quad (1a)$$

First harmonic of the frequency spectrum.

$$\frac{A}{p} = C_1^x \quad (1b)$$

And n-th harmonic of the frequency spectrum is obtained by:

$$\frac{2A}{p}\frac{(-1)^{\frac{n}{2}+1}}{n^2+1}\cos(nw_o t) = C_n^x \quad (1\,c)$$

The signal spectrum of the TV decoder output is decreased by the factor (1/a), in which a is the attenuation factor of higher harmonics to control the ripple in the TV decoder output. Thus, for each frequency between 40 to 60 MHz, where the noise signal spectrum magnitude C_1^x is less that the average noise spectrum magnitude, the output is set to zero.

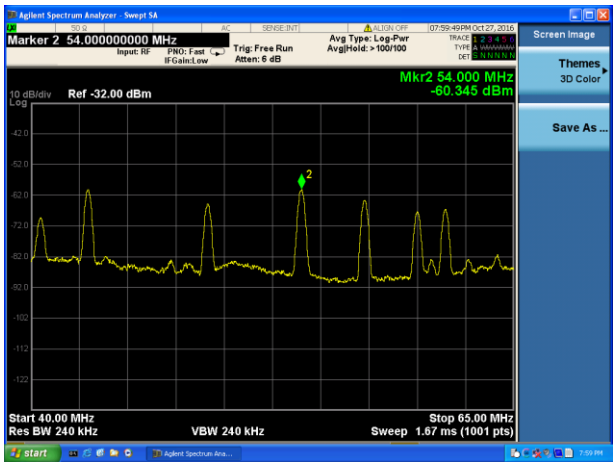

Figure 3. Frequency domain spectrum of the non-filtered TV decoder output voltage.

To achieve an output signal approximately equal to zero, a fourth order Bessel band-stop filter can be implemented. By using the Fourier series in Equation (1), the C_1^y term can be obtained as

$$C_1^y = \frac{A}{4}H(jW_o) \quad (2)$$

where C_1^y is the first harmonic of the frequency spectrum of the TV decoder output, $H(jW_0)$ is the gain of band-stop filter, and A/4 is the first harmonic of frequency spectrum of the TV decoder output. Therefore

$$C_1^y = \frac{1}{2a}\frac{A}{p} \quad (3)$$

The attenuation factor *a* is determined by

$$a = \frac{2C^2R^2\omega^2}{\pi(1+\omega)} \quad (4)$$

where ω is the frequency spectrum of the system, and R,C are the time constants of the cut-off frequencies obtained through the Bessel filter.

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Next, Equation (4) is implemented in the FPGA, which contains methods for the communication with the graphic interface. It allows the control of parameters on the four-order Bessel band-stop filter for the attenuation of the electronic noise of the TV decoder output. This filter embedded in the FPGA has a gain of 10, a minimum cut-off frequency of 40 MHz and a maximum of 60 MHz. It improves the image acquisition through the TV decoder of the FPGA. The Bessel filter is widely used in the industry to implement passive and active analog filters [17]. This filter can increase the flat time and decrease the group delay ripple performance of the filtered signal, as show in Figure 4.

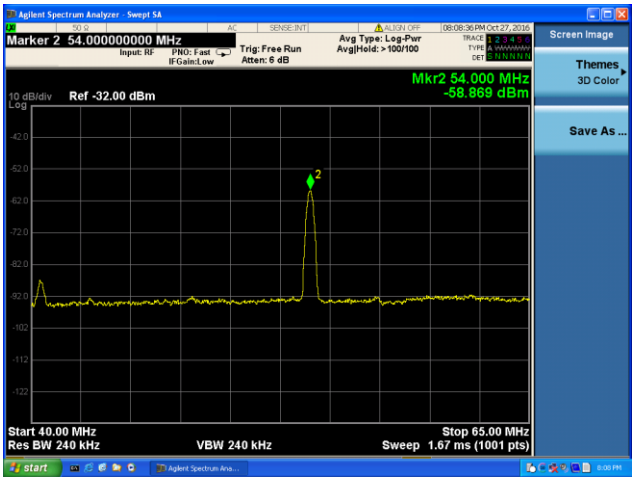

Figure 4. Frequency domain spectrum of the filtered TV decoder output voltage.

Figure 5 shows the experiment setup used to measure the frecuency spectrum of TV decoder output voltages of the FPGA. For this, a N9020A spectrum alalizer (Agilent Technologies®) is used to evaluate the behavior of the TV decoder output voltage at the frecuency domain.

The implemented parameter control in the graphic interface for the filters considers the configuration of the USB connection in the host computer, function filter settings and the procedures to select source signal and filtered output voltage.

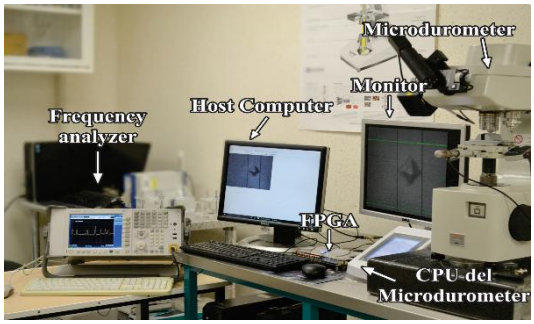

Figure 5. Setup experimental to measure frequency spectrum of TV decoder.

Two variables (Filtered and V) are used to store both filtered and non-filtered TV decoder output voltages values, respectively. Through the function Ain, the analog channel of FPGA is used as source signal, in which the TV decoder output voltages values are assigned to the variable V of the graphic interface.

On the other hand, a function *dspfilter.Filter(V)* includes the parameters of the filter such as the cut-off frequencies, orders and topologies. The filter topologies considered in our graphic interface are the Butterworth, Bessel and Chebyshev ones. These topologies include the following features: minimum cut-off frequency from 0 Hz, maximum cut-off frequency from to 100 Mhz, filters up to eight-order and response types of low-pass, high-pass, band-pass and band-stop. For this research work, we adjusted the parameters of the graphic interface to a fourth-order Bessel band-stop filter and a minimum cut-off frequency of 10 Mhz and a maximum cut-off frequency of 60 Mhz. The Bessel filter is chosen with these features to filter low-frequency noise and to obtain high stability in the real-time image acquisition for hardness tests by indentation.

The figure 6 shows the experimental setup to obtain the real-time image acquisition. This experimental setup includes the graphic interface developed through Delphi Borland 7.net, as well as the FPGA Altera DE2 Board, the microdurometer HM-124, the monitor LCD and the host computer. We applied this setup in particular for indenting an aluminum-nitride-hafmio film with thickness of 1µm.

The host computer communicates with the board through the USB-Blaster link®. The facility can be used to verify the functionality of video components on the board, to store the frames sent from the video-in ports, and to display patterns on the VGA port.

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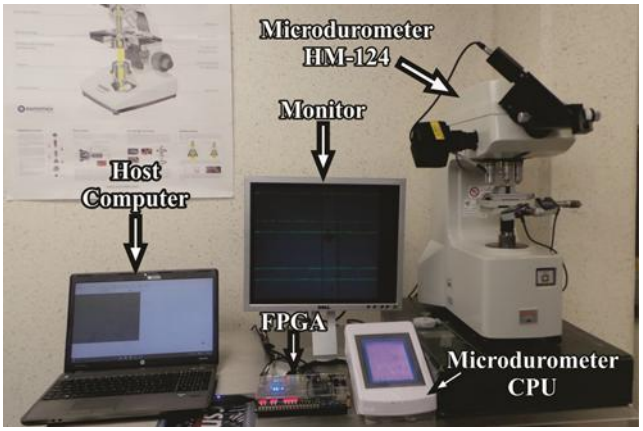

Figure 6. Experimental setup to obtain the real time image acquisition.

The DE2 board includes a 16-pin D-SUB connector for VGA output. The VGA synchronization signals are provided directly from the Cyclone II FPGA, and the analog devices ADV7123 triple IO-bit high-speed video DAC are used to produce the analog data signals (red, green, blue) and support resolutions up to 1600*1200 pixels at 100 MHz.

C. Video camera decoding

We used a charge-coupled device (CCD) camera implemented to the microdurometer model HM-124, with a standard NTSC video output as our video camera input. The image data are read in from the Video-In plug on the DE2 board and go through a set of hardware modules, see Figure 6.

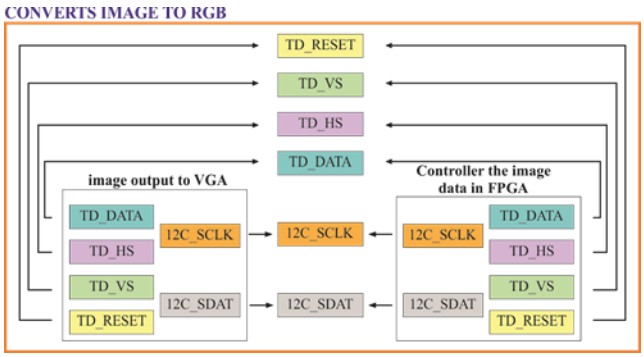

Figure 7. Converting the input data into a standard RGB.

Figure 7 reports the block scheme of the algorithms programed in verilog VHDL: software image output to VGA and controller the image data in FPGA. Both algorithms are connected through a logic gate "or", to controller the same pins physical of the FPGA. The block scheme is formed by the vector TD_DATA with resolution of 8 bits, which will produce the decoding of the image.

They convert the input data into a standard RGB format, which is displayed on a VGA screen. The data obtained directly from the camera are in the ITU656 format, and hence they must first be converted into a more standard YUV 4:2:2 format also referred to as YCbCr. This is a color display format commonly used for encrypting RGB data; where Y represents the luma component, whereas the components Cb and Cr stand for the blue difference and the red difference, respectively, see Figure 8.

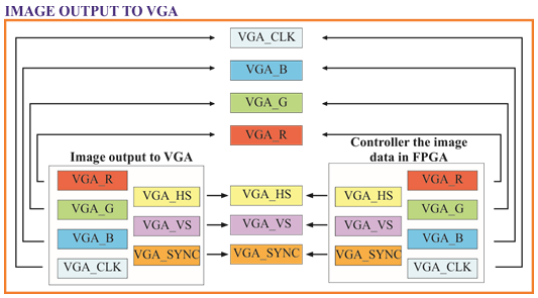

Figure 8. RGB output to VGA.

Figure 8 show the block scheme of the algorithms programed in verilog VHDL: software image output to VGA and Controller the image data in FPGA. Both algorithms are connected through a logic gate "or", to make posible its visualization on a standard VGA screen. The pins VGA_R, VGA_G and VGA_B are connected by a logic gate or programmed in VHDL, which controls the reading of data from the SRAM and to send them to the VGA screen. The block scheme is formed by the vector TD_DATA with resolution of 8 bits, which will produce the decoding of the image. Other logic gate "or", controls the interconnection of the pins VGA_SYNC, VGA_BLANK, VGA_HS and VGA_VS of the modules: software image output to VGA and controller the image data in FPGA.

After being converted, the image data are the supply for an SDRAM FIFO, which acts as a frame buffer. The output of the FIFO is then passed through other conversion process, transforming the data from the YUV 4:2:2 format into the YUV 4:4:4 format. Finally, the new YCbCr formatted image data are converted once more into the standard 10-bit RGB format, in order to make possible its visualization on a standard VGA screen, see Figure 9.

The whole process is utilized by Terasic Instrument's DE2_TV programming code of Altera's DE2 board. This code was modified in such a way that the image acquisition and VGA display (see Figure 10) core are controlled by the host computer, supporting the transfer of data from DE2´s SRAM to PC and vice versa through an USB connection.

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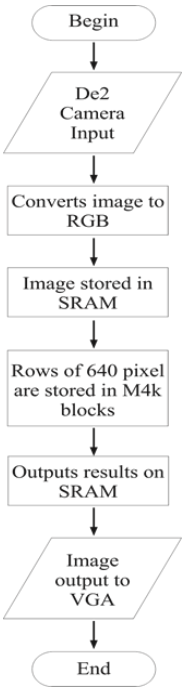

Figure 9. Flow chart of image conversions for displaying the DE2 image on a TV screen.

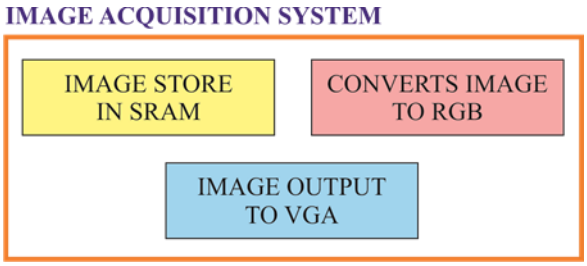

Figure 10. Image acquisition and VGA display.

The video signals decoded from the video decoder chip are interlaced and are transmitted in the form of odd field and even field. Specially, the data format "FF 00 00 SAV" is a time reference code which marks the beginning of effective video data. "Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3 … Cr718 Y719" composes effective video data, which accord with the ITU-R656 standard. "FF 00 00 EAV" is also a time reference code which marks the end of effective video data. The ITU-R656 decoder detects the time reference code "FF 00 00 SAV", generates an effective line signal, and starts to decode the subsequent video data; it converts 8-bit ITU-R656 data into 16-bit YCrCb data.

D. Controlling the image data in FPGA´s memories.

The DE2 board communicates with the graphic interface (see Figure 11). This allows a user to access various components on the board through a USB connection from a host computer. In particular, our aims are placing the image data in SRAM, SDRAM or a Flash memory loading an image to be displayed on a VGA output screen, and introducing into the image a cursor, which can be controlled by means of the x/y-axes scroll bars on the graphic interface. For this, the SRAM controller is responsible for sending the data from the camera to the VGA screen. But these data are sent additionally to SDRAM and to FLASH controllers, which have three user-selectable asynchronous ports, in addition to the host port that provides a link with the command controller. Therefore, the connection between the VGA DAC controller and the FPGA memory allows displaying the image captured by the camera on the VGA screen. The whole image acquisition system is embedded on a FPGA programmed in Verilog HDL, VHDL and block diagram, only making use of the free software Altera´s Quartus II v. 11.1®.

E. SRAM Controller Module.

Through the collection of image capture module and the conversion of image format conversion module, the valid pixels are flown into VGA sequential control module for image show. Due to the different speed between front end and back end, it needs to cache images. With a SRAM + FIFO form, the SRAM controller module mainly includes four FIFO that two is for reading and two is for writing and one SRAM controller. Here, the data port of write FIFO1 is correspond to {1'b0,sCMOS_G[11:7], sCMOS_B[11:2]}, the data port of write FIFO2 is correspond to {1'b0, sCMOS_G[6:2], sCMOS_R[11:2]}.

In other words, the top 10 digits of the 12 digits of the RGB pixels are taken from the image format conversion module, and then three roads of them are merged to two roads of 16 digits signal and transmitted to write FIFO1 and FIFO2. Due to the limited resources on DE2, the SRAM is divided into two areas for reading and writing. In this way, we can perform read/write in double simultaneously and speeding up the transmitting of pixels to VGA sequential control module. The FIFO in this module is instantiated through QUARTUS II.

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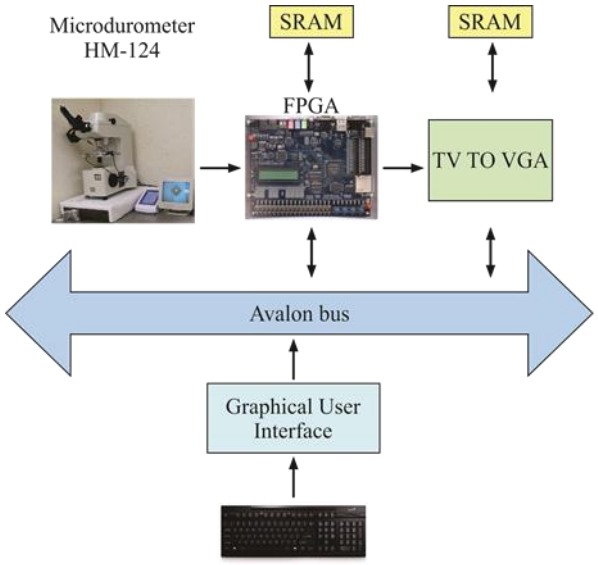

Figure 11. Image acquisition embedded in a FPGA.

The SRAM controller was realized as follows: The pins of the SRAM device are usually divided into three kinds: control pins (OEN, CEN, WEN, LBN, UBN), address pins (ADDR[0:17]), and data pins (DQ[0:15]). Each time before it enters into the normal work state, SRAM needs initialization, which in turn includes a 200 μs stable input. After the mode register is set, SRAM begins to enter into normal work state. First, it enables the line that will write/read. Second, the right column is opened. Then it bursts write/read to the address chosen. In addition, due to the particularity of the SRAM storage structure, we need to rewrite all memories on the original effective line and reset its addresses, which is called precharge, see Figure 12.

Figure 12 show an extension of the block scheme of the algorithms programed in verilog VHDL: software image output to VGA and Controller the image data in FPGA, which the aims of the block scheme are placing the image data in SRAM memory. The module image output to VGA is programed in VHDL, which through a logic gate "or", determine when the module place the image data in SRAM memory. The DQ module determines the read and write times of the SRAM_DQ output. For evaluate these times, is necessary configure the pins SRAM_OE_N, SRAM_CE_N, SRAM_WE_N, SRAM_LB_N, SRAM_UB_N of the RAM memory in accordance of datasheet SRAM[1]. The pins of the memory RAM are connected to a logic gate "nand" for determine reading or writing in the RAM memory. Thus, the nand output is the input signal to the DQ module for detemine the Reading or writing in SRAM memory of the Altera DE2 system.

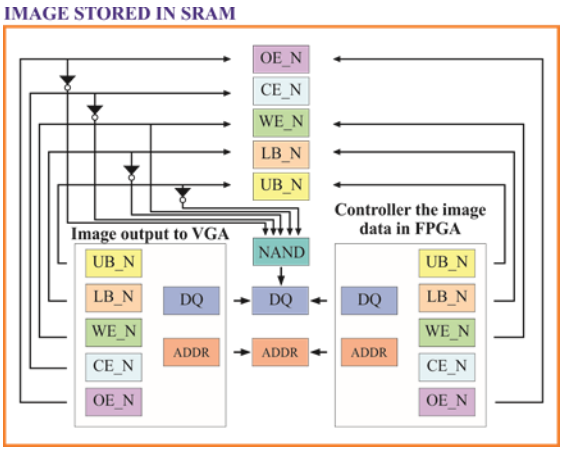

Figure 12. SRAM controller module.

4. Result and discussions

It is important to mention that the indenter measuring system model HM-124 (see Figure 13) does not have the special accessories to change the CCD for enhancing and optimizing the HM-124 test system. Motivated by this lack, we successfully realized real-time image acquisition and VGA display on development boards using the Cyclone II series FPGA on Altera DE2 and interface graphic implemented in Delphi 7.0 net®.

We obtained our final (program) code through compiling, debugging, integrating and downloading all modules to FPGA as described in the previous sections.

Figure 14 shows an image displayed on the TV screen. Several experiments performed in our laboratory showed that our image acquisition system works perfectly well and meets the requirements of real-time image acquisition.

In detail, we used an image acquisition and processing resolution of 640x480 pixels, with sampling rate of 4:1:1, reaching a time to compress an image in the TV decoder (ADV7181B) of about 22ms. The overall efficiency of the system ensures real-time image processing. The occupancy of system resources is shown in Table 1.

ISSN:2319-7900

Figure 13. Microdurometer model HM-124.

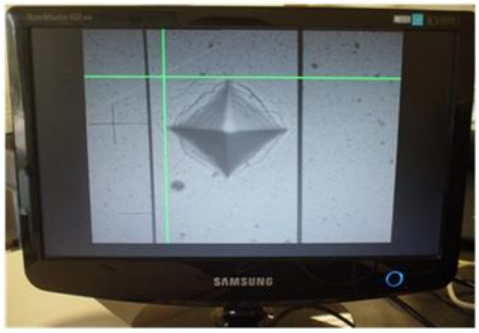

Figure 14. Image displayed on TV screen which is controlled by means of the x/y-axes scroll bars in green color on graphic interface.

Table 1. Occupancy of system resources.

Resource	
Total logic elements	2731/33216
Total registers	1613/33216
Total memory bits	53184/483840
Total Pins	426/475
Embedded Multipliers	4/70
Total PLLs	2/4
Speed	
Average Write Speed	25 MB/S

Furthermore, the power dissipation of our system is of 81.36mW. All parameters were calculated by the Quartus® II software. Besides the display of each image on TV screen, images can be saved as files of commercial format jpeg or bmp, which is achieved by the communication between the board and the host computer via graphic interface. Figure 15 shows a comparison between an indentation footprint image captured directly by a commercial camera (without using our image acquisition system) and the image of the same scene, captured by our system based on FPGA. These two images were obtained during experimental hardness tests with the indenter of microdurometer HM-124, where a force of 0.3kgf was applied to an aluminum-nitride-hafmio film with thickness of 1µm.

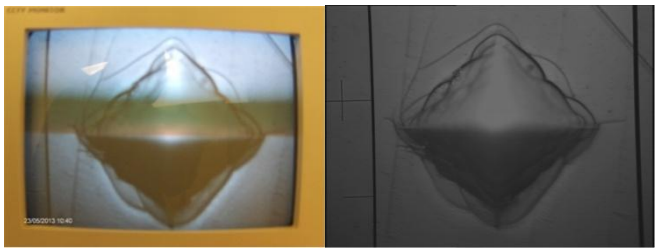

Figure 15. Left: Footprint captured by a commercial camera supplied by the manufacture of the microdurometer HM-124. Right: Footprint stored as JPG image by our image acquisition system.

Figure 16 shows the indentation footprint image captured by the FPGA without signal processing system embedded in it, and the image of the same indentation with the signal processing system embedded in the FPGA, where a force of 0.5kgf was applied to a steel 316 film with thickness of 3mm.

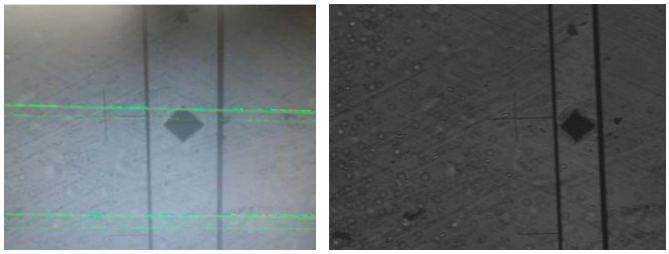

Figure 16. Left: Footprint captured by our image acquisition system without signal processing embedded in a FPGA. Right: Footprint stored as JPG image by our image acquisition system with signal processing embedded in a FPGA.

A special characteristic of our image acquisition and display system consists in the control of the calibration function of the objective lens of the microdurometer. Our system is able to perform real-time adjustment of the focal length of the objectives through a hardness testing machine. The figure shows that for VGA Imaging, through performing long time tests, we observed that the image acquisition and display work perfect, the image captured by the system has a good quality and the system did not produce abnormal phenomena. As a result, we found our system as stable and reliable and satisfying the requirements of real-time image processing.

5. Conclusion

In this work, we presented a high-speed real-time image acquisition system which was developed based on FPGA and using a CCD camera implemented in a microdurometer

model HM-124.The high-speed performance FPGA devices offer a flexible and customizable solution for efficient implementations a wide range of applications. The partial reconfiguration capability of these devices allows utilizing them in a more efficient way. It is also an important feature in reconfigurable computing as it allows quickly swapping modules into and out of the devices without having to reset the complete device for a total reconfiguration. Compared with general PC based image acquisition systems, our system has the distinctive characteristics of small size, low costs, low power consumption, high integration, high-speed and real-time image acquisition. The system performs image acquisition, display on TV screen, and storage of image files having commercial formats (jpeg, bmp). The system has been applied to real-time image acquisition and display in scientific and industrial research. The system's external interface circuit is simple, easy to use, and it is appropriate for transplantation in the control of more camera´s parameters.

Due to its flexibility and high speed performance, future work includes to adapt the system to the environment of industrial manufacturing, in particular with the aim of automatic or semi-automatic hardness tests by indentation, based on digital image analysis.

Acknowledgments

The authors gratefully acknowledge support for this work by the following grants: CONACYT 290733, SEP/CONACYT CB-2011-01-166233, and PROMEP /103.5/13/5701.
ACKNOWLEDGMENT

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