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# Small signal analysis of two stage operational amplifier on TSMC 180nm CMOS technology with low power dissipation

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**Abstract** :In this paper a low voltage two stage Cc miller compensated operational amplifier design is proposed and implemented using 0.18µ micron CMOS process. It discusses low power dissipation ($P_{Diss}$) 0.64mV and gain ($A_V$) 70dB, exhibits a Unity Gain Frequency (UGF) of 3.2599 MHz, phase margin 83.07º and Gain margin 57dB. The design has been carried out in Tanner Tool v14.1 BSIM3v31 model library, Berkeley BSIM3 VERSION 3.1.

Key Terms: Two stage operational amplifier, small signal analysis, AC Analysis, Slew rate, CMOS technology, Miller compensated op-amp, Phase margin Gain margin, Gain Bandwidth, power dissipation.

## 1. Introduction

In current uses of most of consumers, industrial and scientific devices operational amplifier uses very large scale of array. Op-amp architectures that use two or more gain stages [1] are widely used when higher gains are needed. Op-amps are available in many topologies a two stage Op-amp is one of them which is used for high gain amplification [2].

## 2.Block diagram of proposed two stage operational amplifier and operation

The W/L ratios of the transistors are chosen based on the saturation region operation. The first aspect ratios (W/L) of transistors are calculated using the saturation region current equation $I_D$ [1][2][4] .

$$I_D = \beta [(V_{gs} - V_{th}) - (V_{ds}/2)] V_{ds} \quad (1)$$

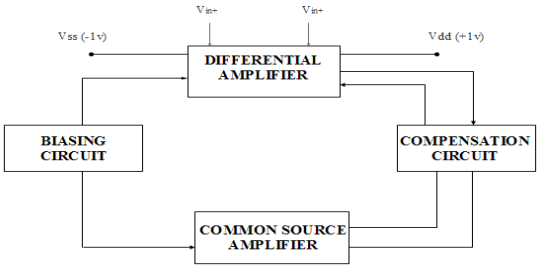


**Figure 1 Proposed block of diagram of two stage Opamp**

Where $\mathbf{I_D}$ is Drain current which is taken as the biasing current, **β is** the process parameters, **(W/L)** is the aspect ratio of a transistor, $\mathbf{V_{gs}}$ is Gate source voltage, $\mathbf{V_{th}}$ is Threshold voltage. $\mathbf{V_{ds}}$ is Drain to Source voltage

Table 1: Modeling of proposed two stage op-amp

| Sn | Parameter | Unit | Main Results |
|---|---|---|---|
| 01 | Compensation capacitor (Cc) | pF | 2.9 ≈ **3** pF |
| 02 | Load capacitor ($C_L$) | pF | 10 pF |
| 03 | Total Drain Current($I_{DD}$) | **µA** | $14.31\times10^{-6}$A |
| 04 | Tail current ($I_5$) | **µA** | **14.31µA** |
| 05 | W/L ratio of first andsecondCMOS | **µs** | 2.9 ≈ **3 µs** |
| 06 | W/L ratio of first andsecondCMOS | **µs** | 2.058 **µs** |

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| | | | |
|---|---|---|---|
| 07 | Tranconductance ($g_m$)for MM1and MM2CMOS | **µs** | 1.8455 **µs** |
| 08 | Saturationvoltage(Dra into source voltage)for MM1 CMOS | **mV** | **$888.9\times10^{-3}$mV** |
| 09 | Saturation voltage (Drain to source voltage) for MM5 CMOS transistor(VDS5) | **mV** | **4.89mV≈5mV** |
| 10 | Gain Bandwidth (GB) | Mhz | 6Mhz |
| 11 | Minimum output voltage(Vminout) | **µV** | 1.11690**µV** |

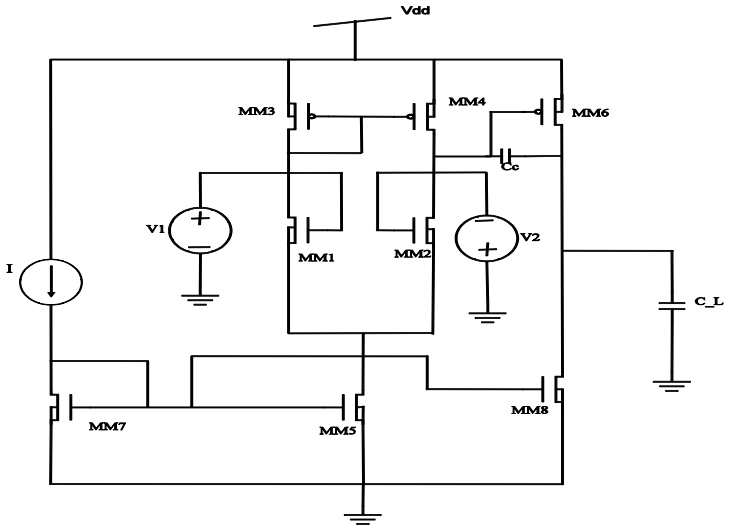


**Figure 2 circuit diagram of propose two stage operational amplifier.**

## 3.Propose circuit diagram of two stage Op-amp

For congenital simply define notation $s_i = (W/L)_i$
Where $s_i$ is aspect ratio of a transistor. We are assume here $\mathbf{g_{m1}=g_{m2}=g_{ml}}$ and $\mathbf{g_{m6}=g_{mll}}$ .

For first step of operational amplifier is to calculate the minimum value of the compensation capacitor $C_C$, We know that placing the output pole $P_2$ 2.2 times higher than the GB(Gain Bandwidth) permitted a 83.07° phase margin (assuming that the RHP zero $Z_1$ is placed at or beyond ten times GB)[3][4] . It was shown that such pole and zero placements result in the following requirement for the minimum value for Cc**:**

$$Cc = 0.22 \text{ X } C_L \qquad (2)$$

Next we need to determine the minimum value for the tail current $I_5$, based on slew-rate requirements. as know as show in Fig(b) the $I_{dis}$ is the drain to source current when the CMOS transistor in saturation region and we know very well that $I_{dis}$ is equal to the summation of $I_{D1}$ and $I_{D2}$ drain to source current which is flow between drain to source when the both CMOS transistor in the saturation region across the MM1 and MM2 transistor so the total amount of $I_{DD}$ is equal to the $I_{DD} = I_{D1} + I_{D2}$ (3)

$$I_{D1} = \beta_1[(V_{gs1} - V_{th1}) - (V_{ds1}/2)]V_{ds1} \qquad (4)$$

$$I_{D2} = \beta_2[(V_{gs2} - V_{th2}) - (V_{ds2}/2)]V_{ds2} \qquad (5)$$

So the total amount of $I_{DD}$ will be summation of $I_{D1}$ and $I_{D2}$ .

### 3.1 Slew Rate

Slew rate can only occur when the differential input signal is large enough to cause *ISS* (*IDD*) to flow through only one of the differential input transistors.[2]

$$SR = \frac{Iss}{CL} = \frac{IDD}{CL} \qquad (6)$$

Then the tail current will be $I_5 = SR \times C_C$

The aspect ratio of MM3 CMOS Transistor can now determined by using the requirement for positive input common-mode range.

$$S3 = (W/L)3 = \frac{I5}{K'[VDD - Vin(max) - VOT03max + VTmax]}$$

$$S3 = \left(\frac{W}{L}\right)3 \qquad (7)$$

$$S_3 = S_4 \qquad (8)$$

The transconductance of the input Cmos transistor can be determine with the help of $V_{DS1}$(Drain to source voltage of MM1 Transistor) and $\beta_1$(The process parameters of MM1 Transistor) and represented by as [4][3]:

$$g_{m1} = \beta_1 \times V_{DS1} \qquad (9)$$

The MM1 CMOS transistor ratio $(W/L)_1$ is directly calculated from $g_{m1}$ which shown below: $S_1=(W/L)_1 = \frac{gm1}{K'1*I5} = S_2$ (10)

Here are enough information available to calculate the saturation voltage of transistor MM5

$V_{DS5}=V_{in(min)}-V_{ss}-\sqrt{\frac{I5}{\beta}}-V_{T1(max)}$ (11)

With the help of $V_{DSS}$ we can determined, (W/L)5 be extracted using the following way :

$S_5 = \frac{I5}{K'(VDS5)^2}$ (12)

Here the first stage of operational amplifier is complited.Next stage is output stage of operational amplifier. For the phase margin of 45.18dB, the location of the output pole was considered to be placed at 2.2 times the gain Bandwidth (GB) then Zero placed at least ten times higher than the GB. [3][4]The transconductance $g_{m6}$ can be determined using

$g_{m6} = 10gm_1$ (13)

for determination of Phase margin , the value of $g_{m6}$ is approximately Ten times the input stage transconductance $g_{m1.}$on this stage two possible approaches to completing the design of MM6.[4][5]Figure of Merit of MOS Transistors can be determine by

GB= $g_{m1}/C_c$ = 6Mhz

As we know that in the Fig(b),the first stage is to achieve proper mirroring of the first stage current mirror load of MM3 and MM4 CMOS Transistor and this requires that [5]:

$V_{GS4} = V_{GS6}$ (14)

Assuming $g_{m6}$ = **11.3 µs** and calculating $g_{m4}$ as :

$g_{m6} = 10 \times GB \times Cc$

$\mathbf{g_{m6} = 6\times10^{-12}}$

Knowing $g_{m6}$ and $s_6$ will define the Dc current $I_6$ using the following equation:

$I_6 = gm_6^2 / 2 \times \mathbf{(k'_6)} (W/L)_6 = 1.08\mu\mathbf{A}$ (15)

The device size of $MM_7$ can be determined from the balance equation given below:

$S_7=(W/L)_7=(W/L)_5\times \frac{I6}{I5}$ (16)

Let's us check the Vmin (out) although the W/L of $MM_7$ is large enough that this is probably not necessary. The value of Vmin (out) is

$V_{min(out)}=V_{DS7(sat)}=\sqrt{\frac{2\times I6}{K\times S7}}$ (17)

$V_{min(out)}$ = 1.11690**µV** ,which is less than required, At this point, the first stage–cut design is completed. Gain margin and Phase Margin [6] :

$PM=\frac{2\times gm2\times gm6}{I5\times(\lambda2+\lambda3)\times(\lambda6+\lambda7)}$ (18)

PM = 83.07°

Here gm2 and gm6 are transconductances of CMOS transistor $MM_2$ and $MM_6$ and $\lambda_2$, $\lambda_3$, $\lambda_6$, $\lambda_7$ are different channel length modulation for n-channel as well as p-channel.

## 4 Power Dissipation

$P_{Diss} = (I_6+I_5)(V_{DD}-V_{SS})$ (19)

Table : 2 Aspect Ratios of the Transistors (W/L)µm for the Two Stage Compensated Op-Amp.

| Transistor | Aspect Ratios (W/L)µm |
|---|---|
| **MM1** | **1/0.18µm = 5.55** |
| **MM2** | **1/0.18µm = 5.55** |
| **MM3** | **1.8/0.18 µm = 10** |
| **MM4** | **1.8/0.18 µm = 10** |
| **MM5** | **3.5/0.18 µm= 19.44** |
| **MM6** | **6/0.18 µm= 27.44** |
| **MM7** | **3.5/0.18µm= 19.44** |
| **MM8** | **4.5/0.18 µm=25** |

5. Implemented Results

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The two stage op-amp is simulated using the 0.18µm CMOS technology. The transient analysis for the op-amp circuit is taken for 1V p-p differential voltage and Gain Bandwidth 6 MHz.

The phase margin analysis of the two stage op-amp circuit is shown in figure(c).

## 4.1 A. C. Analysis

Phase Margin: Phase margin of proposed Op-amp is 83.07º.

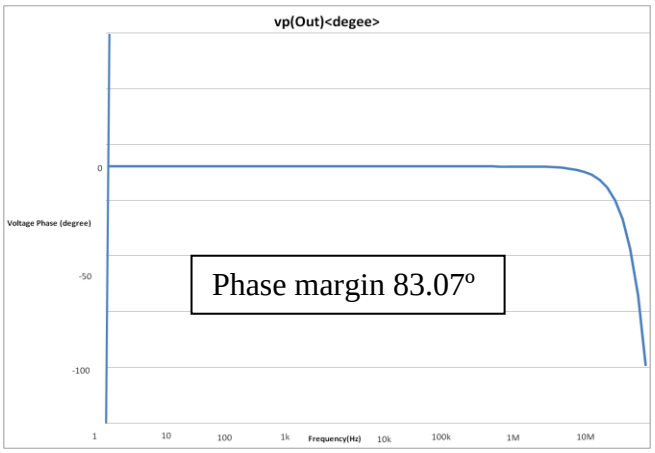


Figure 3 Phase Margin of two stage Op-amp

Gain Margin : Gain margin of proposed two stage Op-amp is 57dB.

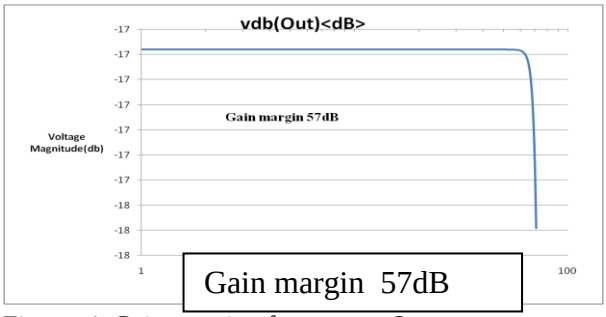


Figure 4 Gain margin of two stage Op-amp

5.2 Slew Rate analysis

Slew rate of proposed Op-amp is 6.051V/**µs**

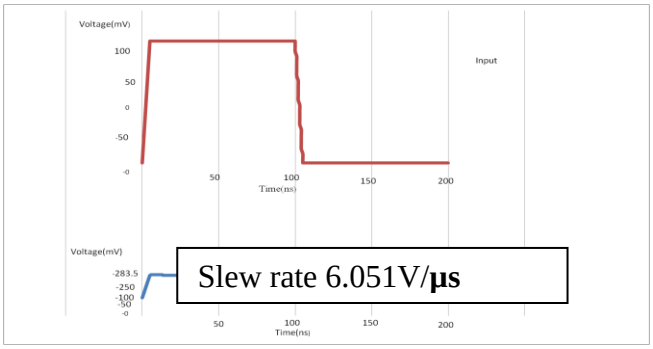


Figure 5 Slew Rate of two stage op-amp

5.3 PSRR (Power Supply Rejection Ratio)

Power Supply Rejection Ratio of proposed op-amp is 0.64mV.

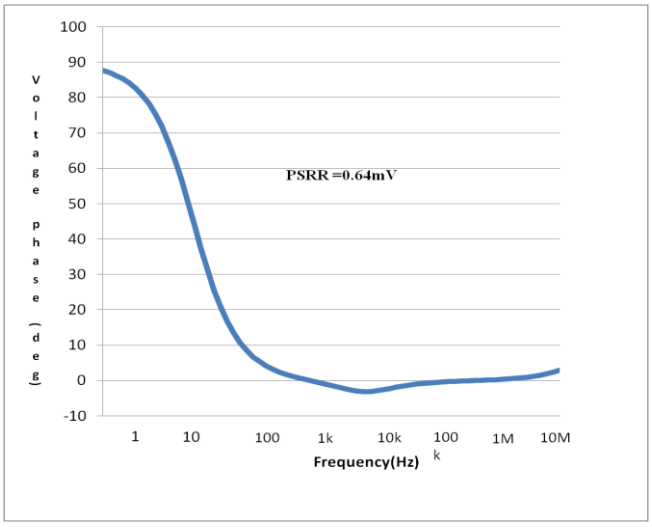


Figure 6 PSRR of two stage op-amp

Table 3 Performance Summary of the Op-Amps

| Parameters | Performance on the bases of 0.18µm CMOS Technology |
|---|---|
| Gain (dB) | 70dB |
| Gain margin (dB) | 45dB |
| Phase Margin (º) | 83.07º |

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| | |
|---|---|
| Bandwidth (MHz) | 7.565Mhz |
| Power Dissipation | 15.39mwatt |
| Power Supply Rejection Ratio (mV) | 0.64mV |
| Slew Rate (V/ µs) | 6.051V/µs |

## Conclusions

Two stage operational amplifier using 0.18µ CMOS technology on Millers compensation capacitor (Cc) with 10kohm Register (R) with parallel based on compensation of right half plane Zero. A carefully and wide analysis are required to get good exertion and desired results. The gain Bandwidth (GB) which is a constant make remonstrance to the designing the circuits for high DC gain and high bandwidth applications. The improvement in unity gain bandwidth has been done by increasing the bias current up to 14.31µamp which decreases the DC gain and increases the power dissipation at the 0.64mv, still provides a good alternative control for an operational amplifier to operate at a high frequency avoid the white noise and short noise which is occur with increasing resister (R) values.

### 6.Acknowledgment

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