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Design of Convolution Encoder Time Domain approach

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Abstract Channel coding deals with error control techniques. If the data at the output of a communications system has errors that are too frequent for the desired use, the errors can often be reduced by the use of a number of techniques. When the errors introduced by the information channel are unacceptable then the channel coding is needed. The use of channel coders with source coders provides the efficient and reliable transmission in the presence of noise. Coding permits an increased rate of information transfer at a fixed error rate, or a reduced error rate for a fixed transfer rate. A convolution coder accepts a fixed number of message symbols and produces a fixed number of code symbols, but its computations depends not only on the current set of input symbols but also on some of previous input symbols.[1] Through this paper we have illustrated design of convolution encoder using time domain approach with VHDL platform.

Keyword : VHDL

I Introduction

A convolution code was introduced in 1955. In convolutional code, the block of *n* code digits generated by the encoder in a particular time limit, depends not only on the block of *k* message digits within that time unit but also on the data digits within a previous span of N-1 time unit (N>1). For convolutional codes, *k* and *n* are usually small. Convolutional codes can be devised for correcting random errors, burst errors or both. Encoding is easily implemented by shift registers [2].

II Background

The time domain behavior of a binary convolution encoder with code rate 1/M may be defined in terms of set of **M impulses response.** The simple encoder of fig[] having code rate ½.Hence,we need two impulse responses to characterize its behavior in the time domain. Let the sequence $[g_0^1, g_1^1, \ldots\ldots, g_x^1]$ {Here ,x represents the number of points from where bits are extracted for modulo-2-adders}denotes the impulse response for path p1 and the sequence $[g_2^2, g_2^2, \ldots\ldots, g_x^2]$denotes the impulse response of path p2.There two impulse responses are obtained by determining the two output sequence of the encoder that are produced in response to the input sequence (1,0,0,…..).The impulse response so defined is called the generator sequence of the code.

Let (d_0, d1,d2,…..)denote the message sequence that enter the encoder of fig[] one bit at a time (starting with d_0).The encoder generates the two output sequence ,denoted by $[C_i^1]$ and $[C_i^2]$,by convolving the message sequence with the impulse response of path p1 and p2 respectively.Thus,the output sequence of path p1 is defined by **convolution sum:**

$$C_i^{(1)} = \sum_{i=0}^{x} g_i^{(1)} d_{i-1},\ i=0,1,2,\ldots\ldots\ldots$$

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Where, $d_{i-1} = 0$ for all $l > i$.

Likewise, the output sequence of path P2 is described by

$C_i^{(2)} = \sum_{i=0}^{x} g_i^{(2)} d_{ie-1}$, i=0,1,2,……..

After convolution, the two sequences $[C_i^{(1)}]$ and $[C_i^{(2)}]$ are combined by the multiplexer to produce the encoder output sequence $[C_i]$, as shown by

$[C_i] = [C_0^{(1)}, C_0^{(2)}, C_1^{(1)}, C_1^{(2)}$…….].[4]

III Proposed work

The following example illustrates the steps to obtain control bits in convolution code.

The sample impulse responses are considered.

Impulse response of path P1 is

$g_i^{(1)} = [g_0^{(1)}, g_1^{(1)}, g_2^{(1)}] = [1, 1, 1]$ ……..(1)

And Impulse response of path P2 is

$g_i^{(2)} = [g_0^{(2)}, g_1^{(2)}, g_2^{(2)}] = [1, 0, 1]$ ……..(2)

Note that the generator sequence or impulse response is directly obtained from circuit diagram of encoder '1' is representing a 'connection' and a '0' is representing 'no connection' with the modulo-2 adder determining the sequence for that path.

Let the incoming message sequence be as follows:

(d0, d1, d2, d3, d4) = (1 0 0 1 1)

Then, the use of equation (1) yields the following values for the elements that constitute the path P1 output sequence:

$C_0^{(1)} = g_0^{(1)}d0 = 1*1 = 1$

$C_1^{(1)} = g_0^{(1)}d1 + g_1^{(1)}d0 = 1*0 + 1*1 = 1$

$C_2^{(1)} = g_0^{(1)}d2 + g_1^{(1)}d1 + g_2^{(1)}d0 = 1*0 + 1*0 + 1*1 = 1$

$C_3^{(1)} = g_0^{(1)}d3 + g_1^{(1)}d2 + g_2^{(1)}d1 = 1*1 + 1*0 + 1*0 = 1$

$C_4^{(1)} = g_0^{(1)}d4 + g_1^{(1)}d3 + g_2^{(1)}d2 = 1*1 + 1*1 + 1*0 = 0$

$C_5^{(1)} = g_1^{(1)}d4 + g_2^{(1)}d3 = 1*1 + 1*1 = 0$

$C_6^{(1)} = g_2^{(1)}d4 = 1*1 = 1$

Hence the output of path P1 is $[C_i^{(1)}] = [1\ 1\ 1\ 1\ 0\ 0\ 1]$

Similarly, equation (2) yields the following output for path P2,

$C_0^{(2)} = g_0^{(2)}d0 = 1*1 = 1$

$C_1^{(2)} = g_0^{(2)}d1 + g_1^{(2)}d0 = 1*0 + 0*1 = 0$

$C_2^{(2)} = g_0^{(2)}d2 + g_1^{(2)}d1 + g_2^{(2)}d0 = 1*0 + 0*0 + 1*1 = 1$

$C_3^{(2)} = g_0^{(2)}d3 + g_1^{(2)}d2 + g_2^{(2)}d1 = 1*1 + 0*0 + 1*0 = 1$

$C_4^{(2)} = g_0^{(2)}d4 + g_1^{(2)}d2 + g_2^{(2)}d2 = 1*1 + 0*1 + 1*0 = 1$

$C_5^{(2)} = g_1^{(2)}d4 + g_2^{(2)}d3 = 0*1 + 1*1 = 1$

$C_6^{(2)} = g_2^{(2)}d4 = 1*1 = 1$

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Hence the output of path P2 is $[C_i^{(2)}]$ = [1 0 1 1 1 1 1]

Finally, multiplexing $[C_i^{(1)}]$ and $[C_i^{(2)}]$, we get the encoded output, sequence as

$[C_i]$ = [11, 10, 11, 11, 01, 01, 11]

Note that the message length k=5, which produces M(K + L – 1) = 2(5 + 3 – 1) = 14 bits output sequence.[4]

IV Experimental Results

In this section RTL for above example obtained by coding in VHDL is shown.

Simulation results are also given so as to get verification

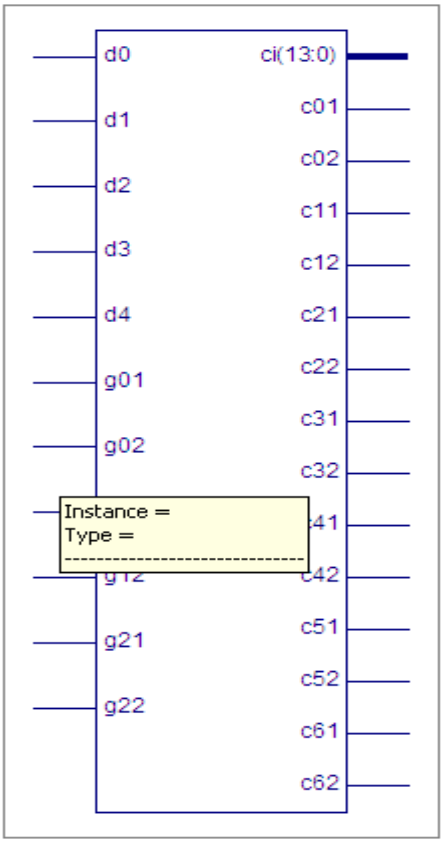

Fig 3.1 RTL Convolutio Encoder entity

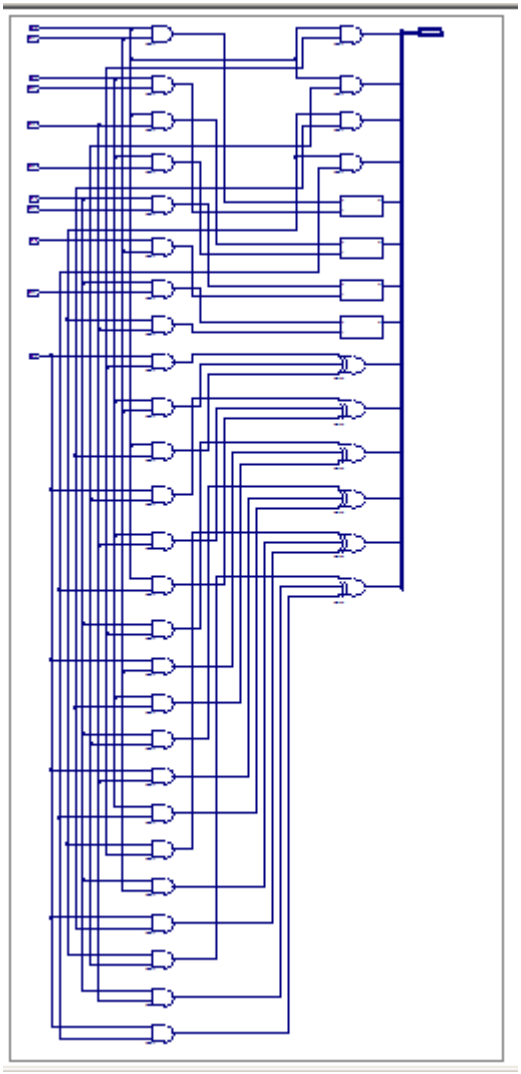

Fig 3.2

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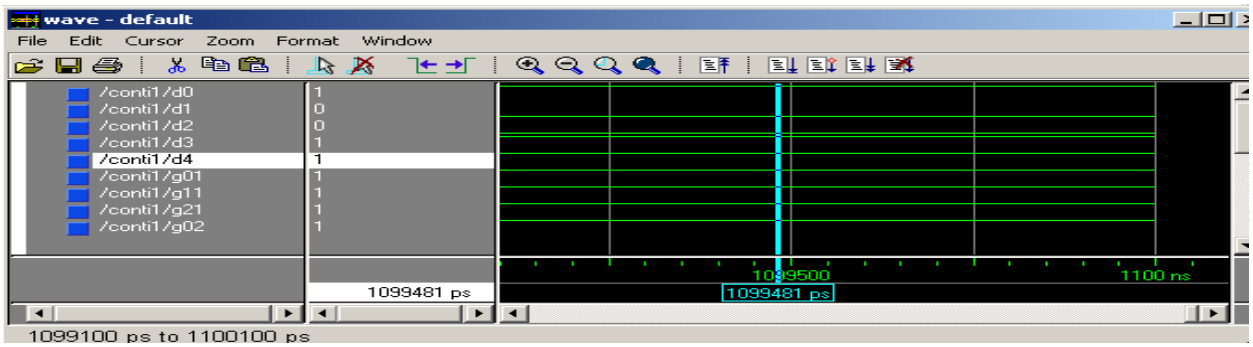

Fig 4.1 Simulation Result

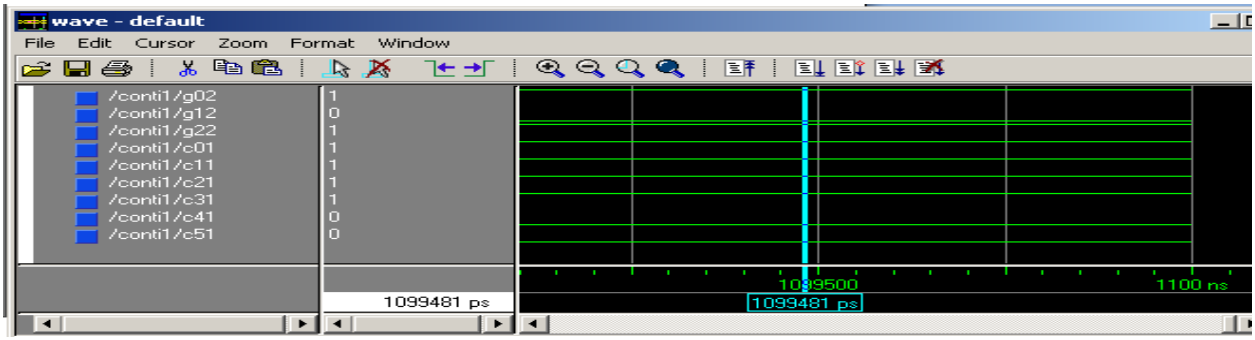

Fig 4.2 Simulation result

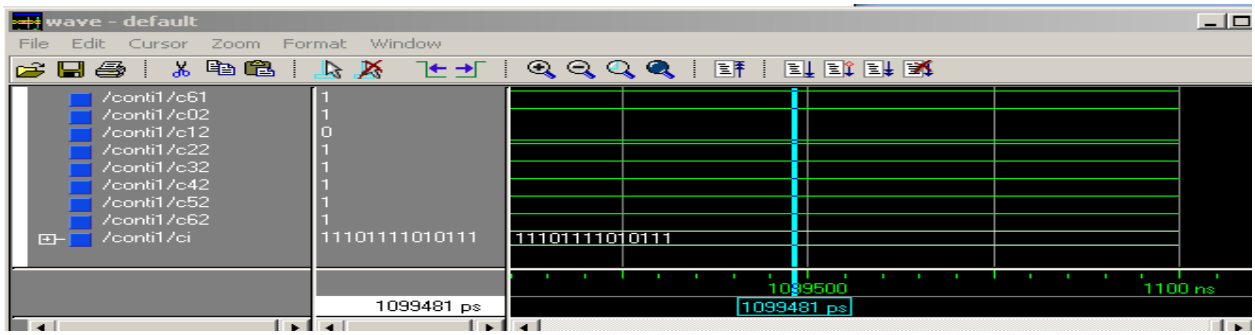

Fig 4.3 Simulation Result

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V Conclusion

Convolution encoder can be designed for various impulse responses for n no. of bits using time domain method.. For single bit input multi bit output sequence can be generated specially useful when large BW is acceptable.

VI REFERENCES

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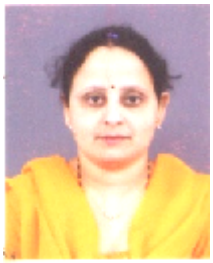
[3] "A Viterbi Decoder Using System C for Area Efficient VLSI Implementation" Thesis by Serkan Sozen

VII Biography



Mrs Supriya P K urlekar (ME)working asAsst.prof in SITCOE Yadrav.

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