International Journal of Advanced Computer Technology (IJACT)

ISSN:2319-7900

EFFECT OF TEMPERATURE AND THRESHOLD VOLTAGE ON SUB THRESHOLD LOGIC FAMILIES

Isha Arora
M.Tech Student, IMS Engineering College, Ghaziabad, UP
ishaarora64@gmail.com

ABSTRACT- The increasing demand for portable applications has caused a significant growth of low-power design, from system level to device level. To improve switching performance of the subthreshold logic family with comparable energy/switching, we propose the use of sub-DTMOS (sub-threshold Dynamic Threshold MOS) transistors. As per the requirement in applications using ultra low power spectrum these logic families are preferred. Basically, in this paper the effect of temperature and voltage variations are analyzed, while comparing sub threshold logic families sub DT MOS and VT sub CMOS.

Keywords - Sub DT CMOS, VT Sub CMOS.

1. INTRODUCTION

Digital sub-threshold logic circuits have recently been proposed for applications in the ultra-low power end of the design spectrum, where the performance is of secondary importance. Different logic families have been identified as suitable for designing more robust and energy efficient sub-threshold circuits with some tradeoff. Some of them are Sub-threshold CMOS logic, Sub-threshold pseudo-NMOS logic, Variable threshold voltage (VT) sub-threshold CMOS logic, Sub-threshold DTMOS logic, Sub-threshold Domino logic. Specifically we are focusing on two of them, DT CMOS and VT sub CMOS. The effect of temperature and the voltage is the

2. VT SUB CMOS

To ensure proper operations under different temperature and process variations, two sub-threshold logic families, namely, Variable Threshold voltage Sub-threshold CMOS logic (VT-Sub-CMOS logic) and Sub-threshold Dynamic Threshold voltage logic (Sub-DTMOS logic) have been proposed . Both logic families show a significant improvement in stability to temperature and process variations while maintaining the same ultra low-power design constraint. VT-Sub-CMOS logic is sub-CMOS logic with an additional stabilization scheme. The stabilization circuit monitors any change in the transistor current due to temperature and process variations and provides an appropriate bias to the substrate.

In fig 1. The circuit for VT sub CMOS is shown along with an external circuit that is substrate bias stabilization scheme.

There are two main components of the stabilization module in the VT-Sub-CMOS logic, namely, the leakage current monitor (LCM) and self-substrate bias (SSB) circuit (Fig. 2). LCM is used as a leakage current sensor and a control to the SSB circuit. It senses any fluctuation in the transistor current and activates the SSB circuit which then applies an appropriate bias to the substrate of the transistors.

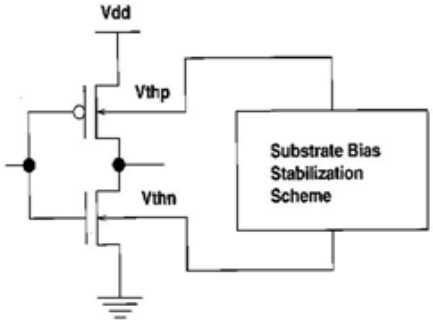


Fig.1 VT Sub CMOS Logic

The circuit for LCM used in here and works well for strong inversion operation but not in the subthreshold region of operation.

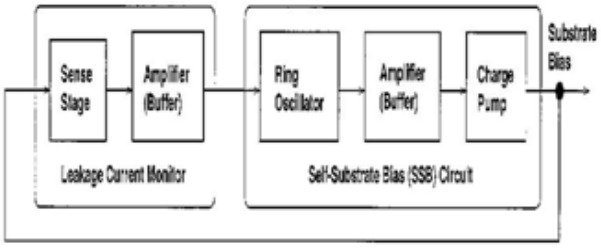


Fig 2. Elements of stabilization scheme.

ISSN:2319-7900

The new LCM circuit used for stabilization in the subthreshold logic is shown in Fig. 3. Leakage currents in PMOS and NMOS transistors are monitored separately. The conductivity of the sensor transistor in the LCM changes with temperature and process variations resulting in a change in output voltage, $V_{control}$. This change in the output voltage is detected and amplified by a buffer circuit, which is used to activate the SSB circuit. Once activated, the SSB circuit then supplies a bias voltage to the substrate V_{bb} and restores the transistor conductivity back to its original value.

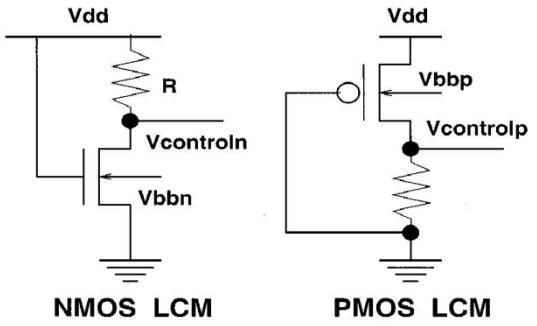


Fig. 3 Leakage Current monitors

And Fig. 4 shows the SSB circuit contains a charge pump which is powered by pulses generated from a ring oscillator. The charge accumulated from the pump is used to bias the substrate of the transistors. The SSB circuit works intermittently and is activated by LCM whenever necessary.

Once the required substrate bias is provided, the SSB circuit is deactivated by LCM. The LCM component thus acts as a thermostat which regulates the fluctuations due to temperature and process variations within a pre-specified tolerable range.

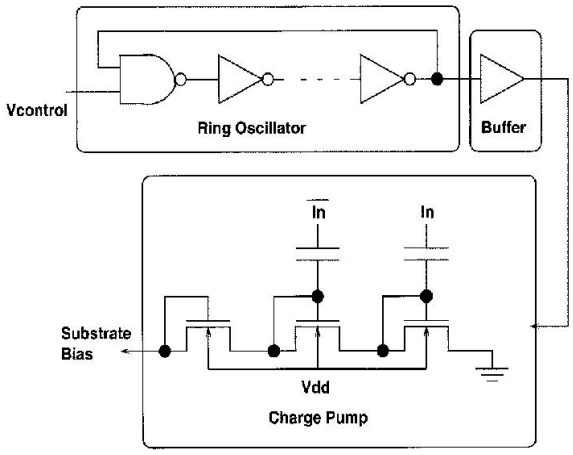
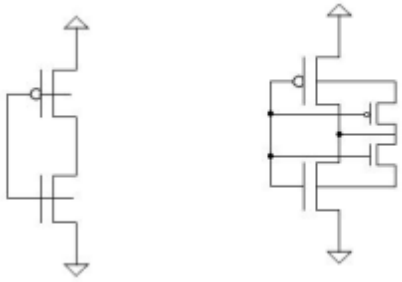


Fig 4. Self-substrate bias circuit.

3. SUB DT CMOS

Sub-DTMOS logic provides an alternative way to achieve the same stability with direct substrate biasing without using additional control circuitry as in the case of VT-sub-CMOS logic. Sub-DTMOS logic uses transistors whose gates are tied to their substrate. In this work we propose a new scheme of high speed, low power inverter using sub-threshold DTMOS transistors, and compare the power efficiency characteristics and temperature stability of proposed design to other schemes by SPICE simulation process technology. DTMOS logic uses transistors whose gates are tied to their substrates (Fig. 5.a) .However; in standard DTMOS topology the body-drain capacitor forms a Miller capacitance that may eliminate any gain from added current drive.



(a) (b)

Fig 5. (a)Standard DT-CMOS

(b) DT-CMOS with augmenting devices

In this section, some different styles of DTMOS transistors (Fig. 5) are used in sub-threshold inverters. Standard DTMOS logic uses transistors whose gates are tied to their substrates (Fig. 1.a) As the substrate voltage in sub-DTMOS logic changes with the gate input voltage, the threshold voltage is dynamically changed. In the off-state, i.e., $V_{in}=0 (V_{in}=V_{dd})$ for NMOS (PMOS), the characteristics of DTMOS transistor is exactly the same as regular MOS transistor. In the on-state, however, the substrate-source voltage (V_{bs}) is for-ward-biased and thus reduces the threshold voltage of DTMOS transistor. The second style of DTMOS uses minimum-sized auxiliary devices to augment the current drive by manipulating the body bias (Fig. 5.b). In this style any excess current caused by forward biasing is used to charge/discharge the output.

The power-delay product (PDP) is a measure of the amount of energy/switching and can be used to determine whether the increase of power consumption is more dominant than the delay improvement, or vice-versa.

4. RESULT

ISSN:2319-7900

A. *Temperature Variations*

In this section the stability of sub-threshold DT-CMOS logics to temperature variation is shown. We analyze the effects of temperature on power and delay of both previously reported and the proposed scheme of sub-DT-CMOS inverter chains. The effect of temperature variation is analyzed using SPICE simulation with Vdd=0.2 V and the temperature parameter is being swept from room temperature (25C) to (125C). For a temperature change from 25C to 125C, the delay of proposed design changes by 64.55%. Standard sub-threshold DT-CMOS shows a change of 62.12% in its delay, so applying the new design to sub-threshold logics does not degrade the stability of circuit to temperature variation significantly. Also VT sub CMOS provens to be better than Sub DT CMOS under the effect of temperature.

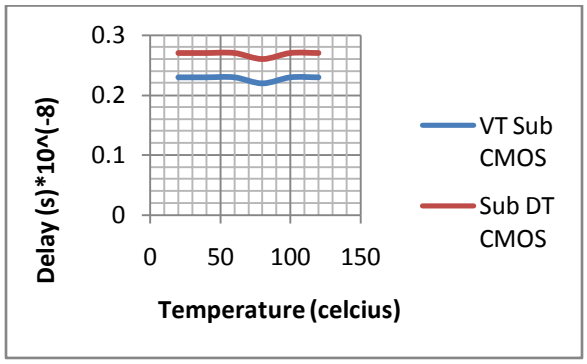


Fig. 4 Delay Vs temperature

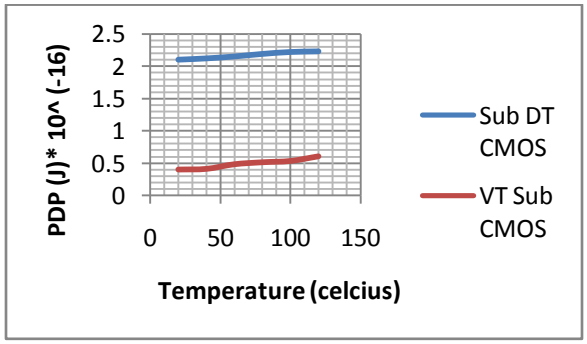


Fig. 5 PDP Vs temperature

B. Threshold Voltage Variations

The effect of process variations on VT-sub-CMOS, and sub-DT-CMOS logic are analyzed by varying the threshold voltages of both NMOS and PMOS by ± 10% from their original designed values. show the delay and power-delay product, respectively, of VT-sub-CMOS, and sub-DT-CMOS logic. The inherent robustness of sub-DT-CMOS and VT-sub-CMOS logic is again observed to be much higher than that of regular sub-CMOS logic.

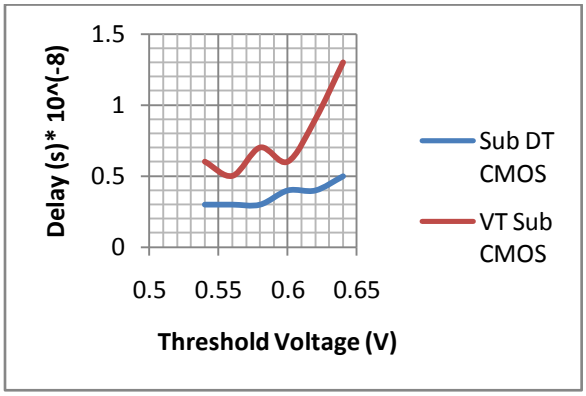


Fig 6. Delay Vs Threshold Voltage

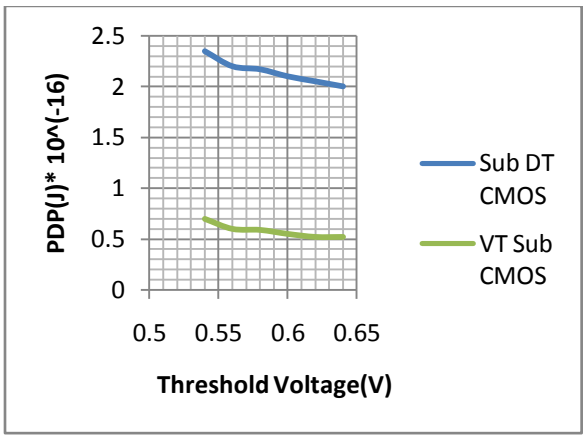


Fig 7. PDP Vs Threshold Voltage

5. Conclusion

We have proposed a new schemes of sub threshold logic families VT sub CMOS and Sub DT-CMOS for sub-threshold logic applications. The delay and PDP of the new scheme were evaluated by SPICE simulations. These schemes shows improved power efficiency for sub-threshold applications. The delay variation of the proposed scheme with temperature was also investigated.

Comparing both VT-sub-CMOS and sub-DTMOS logic families we get to see VT sub CMOS show superior robustness and tolerance to temperature. Although the stability of proposed design to temperature variation was not as well as standard sub-threshold DT-CMOS, but in general the design shows good characteristics in ultra-low power and high speed applications. Also the additional increase

ISSN:2319-7900

in area and process complexities for sub- DTMOS logic is compensated by its higher operating frequency while maintaining comparable energy/switching as regular subthreshold CMOS logic.

REFERENCES

1. S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. Das, W. Haensch, E. J. Nowak, D. M. Sylvester, "Ultralow-voltage, minimum-energy CMOS," IBM Journal of Research & Development, Vol. 50, Issue 4/5, pp. 469-490, Jul/Sep2006.

2. Vishal Sharma, Sanjay Kumar, "Design of Low-power CMOS Cell Structures Using Sub-threshold Conduction Region," International Journal of Scientific & Engineering Research, vol. 2, issue 2, February-2011.

3. H. Soeleman and K. Roy, "Digital CMOS logic operation in the sub threshold region," in Proceedings of the 10th IEEE Great Lakes Symposium on VLSI (GLSVLSI '00), pp. 107–112, Chicago, Ill, USA, March 2000.

4. Ramesh Vaddi, S. Dasgupta, and R. P. Agarwal, "Review Article: Device and Circuit Design Challenges in the Digital Subthreshold Region for Ultralow-Power Applications," Hindawi Publishing Corporation, VLSI Design, Vol. 2009, Article ID 283702.

5. Yehea I. Ismail and Eby G. Friedman, "Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits," IEEE transactions on VLSI Systems, vol.8, No.2, pp.195-206, April2000.